REMARKS

Claims 41, 45, 47, 50 and 52 are amended. Claims 53-70 are cancelled. Claims 41 and 43-52 are pending in the application.

Claims 63-70 stand rejected under 35 U.S.C. § 112, first paragraph. Without admission as to the propriety of the Examiner's rejection, claims 63-70 are cancelled.

Each of claims 41 and 43-62 stand rejected under one or both of 35 U.S.C. § 102 and 35 U.S.C. § 103 over one or more of the following references: Kurimoto, U.S. Patent No. 5,306,655; Verhaar, U.S. Patent No. 5,015,598; Hiroki, U.S. Patent No. 5,512,771; Pintchovski, U.S. Patent No. 5,126,283; Brigham, U.S. Patent No. 5,714,413; and Kumagai, U.S. Patent No. 5,430,313. Without admission as to the propriety of any of the Examiner's rejections, claims 53-62 are cancelled. With respect to the remaining pending claims, the Examiner is reminded by direction to MPEP § 2131 that anticipation requires each and every element of a claim to be disclosed in a single prior art reference. The Examiner is further reminded by direction to MPEP § 2143 that a proper obviousness rejection has the following three requirements: 1) there must be some suggestion or motivation to modify or combine reference teachings; 2) there must be a reasonable expectation of success; and 3) the combined references must teach or suggest all of the claim limitations. Claims 41 and 43-52 are allowable over Kurimoto, Verhaar, Hiroki, Pintchovski, Brigham and Kumagai for the reason that the references, individually or as combined, fail to disclose or suggest each and every limitation in any of those claims.

With respect to independent claim 41, the Examiner indicates at page 7 of the present Action, that the claimed subject matter is taught by Kurimoto because "although there is an intervening dielectric layer [in Kurimoto], the sidewall spacers are still formed on

both of the conductive gate electrodes or laterally adjacent the sidewalls" (page 7 of the present Action). The Examiner suggests amending the claim to incorporate the term "directly" as modifier of the term "on" to more clearly indicate the lack of any intervening layer.

Claim 41 has been amended as suggested by the Examiner to recite forming nitride comprising sidewall spacers directly on the gate electrode's sidewalls, the sidewall spacers joining with the gate dielectric layer. As amended, claim 41 further recites a metal comprising conductive gate electrode, and exposing to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers, a portion of the gate electrode laterally adjacent the sidewall spacers being oxidized by the oxidizing conditions. The amendment to claim 41 is supported by the specification at, for example, page 5, line 17 through page 6, line 4. As noted by the Examiner at page 7 of the present action, Kurimoto discloses an intervening oxide material between gate sidewalls and sidewall spacers. Accordingly, Kurimoto does not disclose or suggest the claim 41 recited forming nitride-comprising sidewall spacers directly on sidewalls of a metal-comprising conductive gate electrode, the sidewall spacers joining with a gate dielectric layer, and claim 41 is not anticipated by or rendered obvious Kirimoto.

Verhaar discloses depositing a protective layer 20 which can comprise silicon nitride over substantially vertical parts of a polycrystalline layer 12 (col. 4, ll. 63 through col. 5, ll. 3). Verhaar does not teach or suggest the claim 41 recited forming metal-comprising conductive gate electrode over a dielectric layer or the claim 41 recited forming nitride-comprising sidewall spacers directly on the gate electrode sidewalls. Hiroki discloses formation of oxide films on the surface of a gate electrode 5 (col. 8, ll.3-6). Hiroki further

discloses subsequent deposition of a nitride film 7 over the intervening oxide film 6 (col. 10, ll. 33-36). Hiroki does not disclose or suggest the claim 41 recited forming nitride-comprising sidewall spacers directly on sidewalls of a metal-comprising conductive gate electrode. Pintchovski discloses formation of various gate structures having a polysilicon layer, an aluminum or an aluminum alloy layer over the poly, and in some embodiments a metal nitride layer. Pintchovski does not disclose or suggest the claim 41 recited forming nitride-comprising sidewall spacers directly on the sidewalls of a metal comprising gate electrode.

Brigham discloses forming an oxide layer 24 over a polysilicon gate electrode 23 (col. 3, ll. 31-32 and col. 4, ll. 60). Brigham further discloses subsequent deposition of a nitride layer 25 over intervening oxide layer 24 (col. 4, ll. 64-67). Brigham does not disclose or suggest the claim 41 recited forming nitride-comprising sidewall spacers directly on sidewalls of a metal-comprising conductive gate electrode. Kumagai discloses forming a gate insulating film on the sides of a polysilicon gate electrode 14 (col. 3, ll. 15-19). Kumagai does not disclose or suggest the claim 41 recited forming nitride comprising sidewall spacers directly on sidewalls of a metal comprising conductive gate electrode.

As discussed above, not one of the various cited references relied on by the Examiner discloses or suggests the claim 41 recited forming nitride-comprising sidewall spacers directly on sidewalls of a metal-comprising conductive gate electrode. Accordingly, the references cannot be combined to suggest the claim 41 recited forming a metal-comprising conductive gate over a gate dielectric layer and forming nitride-comprising sidewall spacers directly on the sidewalls of the metal-comprising conductive gate electrode, the sidewall spacer joining with the gate dielectric layer. Accordingly, claim

41 is not rendered obvious by the various cited combinations of Kurimoto, Verhaar, Hiroki, Pintchovski, Brigham and Kumagai and is allowable over these references.

Dependent claims 43 and 44 are allowable over the various cited combinations of Kurimoto, Verhaar, Hiroki, Pintchovski, Brigham and Kumagai for at least the reason that they depend from allowable base claim 41.

As amended, each of independent claims 45 and 50 recite a metal-comprising gate structure having sidewalls and forming non-oxide or oxidation resistant spacers directly adjacent or directly against sidewalls of the metal-comprising gate structure. Each of claims 45 and 50 are allowable over the various cited combinations of Kurimoto, Verhaar, Hiroki, Pintchovski, Brigham and Kumagai for at least reasons similar to those discussed above with respect to independent claim 41.

Claim 47 is amended to provide an improved claim format. Dependent claims 46-49 and 51 are allowable over the various cited combinations of Kurimoto, Verhaar, Hiroki, Pintchovski, Brigham and Kumagai for at least the reason that they depend from corresponding allowable base claims 45 and 50.

As amended, independent claim 52 recites depositing a first barrier comprising an oxidation resistant material, the first barrier contacting a polysilicon portion, an overlaying metal portion, and an interposed reaction barrier portion of a sidewall of a gate structure. Claim 52 further recites depositing a second barrier comprising the oxidation resistant material disposed over the first barrier. The amendment to claim 52 is supported by the specification at, for example, page 5, line 18 through page 6, line 3; page 6, lines 12-14; page 9, line 9 through page 10, line 9; and Figs. 6 and 7. Independent claim 52 is allowable over the various cited combinations of Kurimoto, Verhaar, Hiroki, Pintchovski,

Brigham and Kumagai for at least reasons similar to those discussed above with respect to independent claim 41.

For the reasons discussed above claims 41 and 43-52 are allowable. Accordingly, applicant respectfully requests formal allowance of claims 41 and 43-52 in the Examiner's next action.

Respectfully submitted,

Dated: February 5, 2003 By: Jennifer J Taylor

Jennifer J Taylor, Ph.D.
Reg. No. 48,711

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Inventor..... Pai-Hung Pan
Assignee..... Micron Technology, Inc.
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Examiner ..... Trinh, Michael
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VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO NOVEMBER 5, 2002 FINAL OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

41. (Amended) A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a metal-comprising conductive gate electrode over a gate dielectric layer on a substrate, the gate electrode having sidewalls and an interface with the gate dielectric layer;

forming nitride-comprising sidewall spacers ~~comprising nitride~~ directly on the gate electrode's sidewalls, the sidewall spacers joining with the gate dielectric layer; and

after forming the sidewall spacers comprising nitride, exposing the substrate to oxidizing conditions effective to channel oxidants through the gate dielectric layer and underneath the sidewall spacers joined therewith, wherein a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric layer, is oxidized.

45. (Amended) A semiconductor processing method of forming a conductive gate comprising:

forming a metal-comprising conductive gate structure on a first layer which is disposed on a substrate, the gate structure comprising a gate electrode having sidewalls and an interface with the first layer;

forming oxidation resistant sidewall spacers directly ~~laterally~~ adjacent the conductive gate structure's sidewalls sufficiently to cover all conductive material comprised by ~~comprising~~ the sidewalls, ~~the sidewall spacers comprising an oxidation resistant material~~; and

after forming the oxidation resistant sidewall spacers, conducting an oxidizing step by channeling oxidants through the first layer which is outwardly exposed laterally proximate the oxidation resistant sidewall spacers wherein ~~the oxidation resistant sidewall spacers provide that~~ only a portion of the gate electrode adjacent the oxidation resistant sidewall spacers and at the interface with the first layer, is oxidized.

47. (Amended) The method of claim 45, wherein the gate structure comprises a polysilicon layer, an overlying metal layer, and an electrically conductive reaction barrier layer intermediate the polysilicon layer and the overlying metal layer.

50. (Amended) A semiconductor processing method of forming a conductive transistor gate over a substrate comprising:

forming a dielectric layer on a substrate;

forming a metal-comprising conductive gate structure over the dielectric layer, the gate structure having sidewalls defining a lateral dimension of the gate structure;

forming a non-oxide material over the gate structure and the dielectric layer, the non-oxide material being directly against the sidewalls;

anisotropically etching the non-oxide material to form spacers on the sidewalls, the spacers laterally adjacent the gate structure and joining with the gate dielectric layer ~~thereat~~; and

exposing the substrate to oxidizing conditions effective to oxidize only that portion of the gate structure adjacent the spacers and the dielectric layer.

52. (Amended) A semiconductor processing method of forming a conductive gate comprising:

forming a gate structure atop a substrate having a dielectric layer thereon, at least a portion of the gate structure being conductive, the conductive portion comprising:

a polysilicon layer,

an overlying metal, and

a reaction barrier layer interposed between the polysilicon and the overlying metal;

covering a top and sidewalls of the gate structure with an oxidation resistant material, the sidewalls comprising a polysilicon portion, an overlying metal portion and an interposed reaction barrier portion, said covering comprising:

depositing a first barrier comprising the oxidation resistant material, the first barrier contacting the polysilicon portion, the overlying metal portion, and the interposed reaction barrier portion of the sidewalls, and

depositing a second barrier comprising the oxidation resistant material disposed over the first barrier ~~material~~,

anisotropically etching the oxidation resistant material to a degree sufficient to leave the oxidation resistant material laterally adjacent to and covering all of the sidewalls of the gate structure while exposing the dielectric layer adjacent the gate structure; and

exposing the substrate to oxidation conditions effective to oxidize a portion of the gate structure laterally adjacent the covered sidewalls and adjacent the dielectric layer.

Claims 53-70 are cancelled.

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